CLAIMS

WHAT IS CLAIMED IS:

1. A memory interface circuit comprising:

an address generating unit for outputting an internal address received from a central processor to an external memory as an access address when the internal address is a branch address, and for incrementing the branch address by one at every access cycle and outputting the incremented branch address as the access address until a next branch address is received, said access address being for prefetching instruction data stored in said external memory;

a plurality of prefetch buffers each having a tag register for storing a branch address, and a data register for storing instruction data stored in an area of said external memory designated by the branch address stored in the tag register;

a first address comparing unit for activating a tag hit signal when said internal address coincides with the branch address stored in the tag register;

a data selecting unit for outputting, to said central processor, instruction data read from the data register corresponding to the tag register containing the hit branch address when said tag hit signal is activated, and outputting, to said central processor, instruction data corresponding to the branch address read from said external memory when said tag hit signal is inactivated; and

a main control unit for controlling operation of said address generating unit, said first address comparing unit, and said data selecting unit during a normal operation period in which said central processor outputs internal addresses successively, and wherein

each of said prefetch buffers is assigned to either a first prefetch buffer which is rewritable during said normal operation period or a second prefetch buffer to be disabled for rewrite during said normal operation period and containing in advance a specified

branch address and instruction data stored in an area of said external memory designated by the specified branch address.

2. The memory interface circuit according to claim 1, comprising

a split register in which one of a number of said prefetch buffers to be used as said first prefetch buffer(s) and a number of the same to be used as said second prefetch buffer(s) is registered, wherein

each of said prefetch buffers is assigned to either said first prefetch buffer or said second prefetch buffer during an initial setting period depending on a value of said split register, the initial setting period preceding said normal operation period.

3. The memory interface circuit according to claim 1, wherein

said main control unit receives the branch address through a data bus connected to said central processor and stores the received branch address in the tag register of said second prefetch buffer, and stores instruction data stored in an area of said external memory designated by the received branch address into the data register corresponding to the tag register of said second prefetch buffer during an initial setting period preceding said normal operation period.

4. The memory interface circuit according to claim 3, comprising

a start register to be set by a write from said central processor, wherein

during said initial setting period, said main control unit stores the branch address received through said data bus in the tag register of said second prefetch buffer, and then outputs the branch address stored in the tag register of said second prefetch buffer to said external memory through said address generating unit in response to the set start register, and stores instruction data read from said external memory in the data register corresponding to the tag register of said second prefetch buffer.

5. The memory interface circuit according to claim 1, comprising:

a data buffer for temporarily storing the instruction data prefetched from said external memory according to the access address; and

a second address comparing unit for outputting a prefetch hit signal when said internal address coincides with the access address for prefetching the instruction data from said external memory, wherein

said data selecting unit outputs the instruction data stored in said data buffer to said central processor when said prefetch hit signal is activated, and outputs, to said central processor, the instruction data corresponding to the branch address read from said external memory when said prefetch hit signal is inactivated.

6. The memory interface circuit according to claim 1, comprising

a branch counter for counting a number of times said central processor outputs branch addresses during said normal operation period, wherein

upon determining that a ratio of a number of times at which the branch address stored in the tag register of said first prefetch buffer is hit to a counter value of said branch counter exceeds a predetermined value during said normal operation period, said main control circuit switches the first prefetch buffer to said second prefetch buffer.

7. The memory interface circuit according to claim 6, wherein

each of said prefetch buffers has a recognition flag for indicating which of said first or second prefetch buffer it is used for.

8. The memory interface circuit according to claim 1, comprising

a branch counter for counting a number of times said central processor outputs branch addresses during said normal operation period, wherein

upon determining that a ratio of a number of times at which the branch address stored in the tag register of said second prefetch buffer is hit to a counter value of said branch counter is equal to or less than a predetermined value during said normal operation

period, said main control circuit switches the second prefetch buffer to said first prefetch buffer.

9. The memory interface circuit according to claim 8, wherein

each of said prefetch buffers has a recognition flag for indicating which of said first or second prefetch buffer it is used for.

10. A memory interface circuit comprising:

an address generating unit for outputting an internal address received from a central processor to an external memory as an access address when the internal address is a branch address, and for incrementing the branch address by one at every access cycle and outputting the incremented branch address as the access address until a next branch address is received, said access address being for prefetching instruction data stored in said external memory;

a plurality of prefetch buffers each having a tag register for storing a branch address, and a data register for storing instruction data stored in an area of said external memory designated by the branch address stored in the tag register;

a first address comparing unit for activating a tag hit signal when said internal address coincides with the branch address stored in the tag register;

a data selecting unit for outputting, to said central processor, instruction data read from the data register corresponding to the tag register containing the hit branch address when said tag hit signal is activated, and outputting, to said central processor, instruction data corresponding to the branch address read from said external memory when said tag hit signal is inactivated;

a branch counter for counting a number of times said central processor outputs branch addresses during said normal operation period; and

a main control unit for controlling operation of said address generating unit, said

first address comparing unit, said data selecting unit, and said branch counter during a normal operation period in which said central processor outputs internal addresses successively, wherein:

each of said prefetch buffers is assigned to either a first prefetch buffer which is rewritable during said normal operation period or a second prefetch buffer to be disabled for rewrite during said normal operation period and containing in advance a specified branch address and instruction data stored in an area of said external memory designated by the specified branch address; and

upon determining a ratio of a number of times at which the branch address stored in the tag register of said first prefetch buffer is hit to a counter value of said branch counter exceeds a predetermined value during said normal operation period, said main control circuit switches the first prefetch buffer to said second prefetch buffer.

11. The memory interface circuit according to claim 10, wherein

upon determining a ratio of a number of times at which the branch address stored in the tag register of said second prefetch buffer is hit to a counter value of said branch counter is equal to or less than a predetermined value during said normal operation period, said main control circuit switches the second prefetch buffer to said first prefetch buffer.

12. The memory interface circuit according to claim 11, wherein

each of said prefetch buffers has a recognition flag for indicating which of said first or second prefetch buffer it is used for.